

CLAIMS

What is claimed is:

1. A computerized method for generating a testbench, the method comprising:

5 generating a plurality of test designs, the plurality of test designs having varied characteristics to allow substantial testing of a design automation tool, wherein generating one of the plurality of test designs comprises:

instantiating the I/O structure of a top level module, the top level module having input and output pins;

10 parameterizing a plurality of submodules from a design module library for interconnection with the top level module, the plurality of submodules having input and output lines;

providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to
15 various input and output pins of the top level module.

2. The computerized method of claim 1, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip.

3. The computerized method of claim 1, wherein the design automation tool is used to implement designs on an ASIC.

20 4. The computerized method of claim 1, wherein the design automation tool is an electronic design automation tool.

5. The computerized method of claim 1, wherein the design automation tool is a synthesis or a place and route tool.

25 6. The computerized method of claim 1, wherein providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs.

7. The computerized method of claim 6, wherein inputs comprise input pins of the top level module, submodule output lines, and registers.

30 8. The computerized method of claim 6, wherein outputs comprise output pins of the top level module, submodule input lines, and registers.

9. The computerized method of claim 8, wherein providing logic to interconnect the plurality of parameterized modules further comprises classifying inputs and outputs as clock lines, control lines, and data lines.

10. The computerized method of claim 8, wherein generating one of the plurality of test designs further comprises:

11. The computerized method of claim 10, generating randomized logic to drive outputs.

5 12. The computerized method of claim 10, wherein generating randomized logic comprises directly wiring outputs to inputs, generating a logic expression using inputs, generating a mathematical expression using inputs, or generating decision logic.

10 13. The computerized method of claim 6, wherein parameterizing the plurality of submodules comprises defining interfaces, data width, and the type of signal for input and output lines associated with the submodule.

14. The computerized method of claim 6, wherein submodules comprise adders, phase lock loops, memory, and timers.

15 15. The computerized method of claim 6, wherein generating one of the plurality of test design further comprises selecting a clock structure for each output.

16. The computerized method of claim 15, wherein clock structures include a plurality of synchronous and asynchronous structures.

17. A computer system for generating a testbench, the computer system comprising:

20 memory operable to hold information associated with a design module library;
a processor coupled to memory, the processor configured to generate a plurality of test designs, the plurality of test designs having varied characteristics to allow substantial testing of a design automation tool, wherein generating one of the plurality of test designs comprises:

25 instantiating the I/O structure of a top level module, the top level module having input and output pins;

parameterizing a plurality of submodules from the design module library for interconnection with the top level module, the plurality of submodules having input and output lines;

30 providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module.

18. The computer system of claim 17, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip.

19. The computer system of claim 17, wherein the design automation tool is used to implement designs on an ASIC.

5 20. The computer system of claim 17, wherein the design automation tool is an electronic design automation tool.

21. The computer system of claim 17, wherein the design automation tool is a synthesis or a place and route tool.

10 22. The computer system of claim 17, wherein providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs.

23. The computer system of claim 22, wherein inputs comprise input pins of the top level module, submodule output lines, and registers.

24. The computer system of claim 22, wherein outputs comprise output pins of the top level module, submodule input lines, and registers.

15 25. An apparatus for generating test a testbench, the apparatus comprising:
means for generating a plurality of test designs, the plurality of test designs having varied characteristics to allow substantial testing of a design automation tool, wherein means for generating one of the plurality of test designs comprises:

20 means for instantiating the I/O structure of a top level module, the top level module having input and output pins;

means for parameterizing a plurality of submodules from a design module library for interconnection with the top level module, the plurality of submodules having input and output lines;

25 means for providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module.

26. The computerized method of claim 25, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip.

30 27. The computerized method of claim 25, wherein the design automation tool is used to implement designs on an ASIC.